What is claimed is:

1. An optical signal receiver, comprising:

a photodetector optically coupled to a fiber optic network:

said photodetector converting an optical signal received from the fiber optic network to an electrical input data signal;

a comparator operatively coupled to said photodetector and to a decision threshold input port;

said comparator comparing the electrical input data signal to a decision threshold signal to provide a digital output data signal;

an error detection and correction circuit operatively coupled to said comparator;

said error detection and correction circuit detecting errors in the digital output data signal and correcting detected errors in the digital output data signal;

said error detection and correction circuit also providing an error signal representative of a number of corrected "1"s and number of corrected "0"s in the output data signal; and

a control circuit operatively coupled to said error detection and correction circuit and to the decision threshold input port of said comparator,

said control circuit calculating a relative percentage error indicator based on the error signal and adjusting the decision threshold signal in response to the relative percentage error indicator.

2. The optical signal receiver according to claim 1,

said control circuit changing a rate of the decision threshold adjustment based on the relative percentage error indicator.

3. The optical signal receiver according to claim 1,

said control circuit dynamically adjusting the decision threshold signal in

response to the relative percentage error indicator.

4. The optical signal receiver according to claim 1, said control circuit including:

a microprocessor circuit operatively coupled to said error detection and correction circuit,

said microprocessor circuit performing the relative percentage error indicator calculation, and outputting a digital control signal based on the relative percentage error indicator; and

a digital-to-analog converter operatively coupled to said microprocessor circuit and to the decision threshold input port,

said digital-to-analog converter adjusting the decision threshold signal based on the digital control signal provided by said microprocessor circuit.

5. The optical signal receiver according to claim 1, said control circuit including

a microprocessor circuit operatively coupled to said error detection and correction circuit, said microprocessor circuit performing the relative percentage error indicator calculation, and outputting a control signal based on the relative percentage error indicator; and

a potentiometer operatively coupled to said microprocessor circuit and to the decision threshold input port, said potentiometer generating the decision threshold signal based on the control signal provided by said microprocessor circuit to thereby adjust the decision threshold signal.

6. The optical signal receiver according to claim 1, said control circuit including

a microprocessor circuit operatively coupled to said error detection and correction circuit, and

an RC circuit operatively coupled to said microprocessor circuit and to the decision threshold input port;

said microprocessor circuit performing the relative percentage error indicator calculation, and adjusting the decision threshold signal with a pulse-width modulated signal.

7. The optical signal receiver according to claim 1, wherein said error detection and correction circuit includes an FEC circuit.

8. The optical signal receiver according to claim 1, further comprising:

a clock and data recovery circuit operatively coupled between said comparator and said error detection and correction circuit,

said clock and data recovery circuit providing a data-recovered output signal and a clock signal to said error detection and correction circuit.

9. The optical signal receiver according to claim 2,

said control circuit calculating the relative percentage error indicator according to:

Indicator = Ones/Zeros when Ones/Zeros ≥ 1 and

Indicator = Zeros/Ones when Zeros/Ones ≥ 1

where Indicator = relative percentage error indicator,

Ones = the number of corrected "1"s in the output data signal, and

Zeroes = the number of corrected "0"s in the output data signal.

10. The optical signal receiver according to claim 9,

said control circuit setting the stepsize amount to a minimum value when the Indicator is below a first threshold value.

11. The optical signal receiver according to claim 9,

said control circuit setting the stepsize amount to a maximum value when the Indicator is above a first threshold value and when

$$|Ones - Zeros| > SecondThreshold\ .$$

12. The optical signal receiver according to claim 9,

said control circuit setting the stepsize amount to a maximum value when the Indicator is above a first threshold value and when

$TotalCount > ThirdThreshold$

where TotalCount = Ones + Zeros.

13. A method of reducing bit errors in a digital data output signal output from an optical receiver having a comparator comparing an input data signal from an optical-to-electrical signal converter to a decision threshold signal to provide the digital output data signal, the method comprising:

inputting a number of corrected "1"s and a number of corrected "0"s corrected in the output data signal;

calculating a relative percentage error indicator based on the number of corrected "1"s and the number of corrected "0"s in the output data signal; and

adjusting the decision threshold signal in response to the calculated relative percentage error indicator.

14. The method of reducing bit errors according to claim 13, further comprising:

changing a rate of said decision threshold adjustment based on the calculated relative percentage error indicator.

15. The method of reducing bit errors according to claim 13, further comprising:

repeating said inputting, calculating and adjusting to dynamically adjust the decision threshold.

16. The method of reducing bit errors according to claim 13,

said adjusting step changing the decision threshold by a stepsize amount in

response to the calculated relative percentage error indicator.

17. The method of reducing bit errors according to claim 13,

said calculating step calculating the relative percentage error indicator according to:

Indicator = Ones/Zeros when Ones/Zeros ≥ 1 and

Indicator = Zeros/Ones when Zeros/Ones ≥ 1

where Indicator = relative percentage error indicator,

Ones = the number of corrected "1"s in the output data signal, and

Zeroes = the number of corrected "0"s in the output data signal.

18. The method of reducing bit errors according to claim 17,

said adjusting step changing the decision threshold by a stepsize amount in response to the calculated relative percentage error indicator.

19. The method of reducing bit errors according to claim 18, further comprising:

setting the stepsize amount to a minimum value when the Indicator is below a first threshold value.

20. The method of reducing bit errors according to claim 18, further comprising:

setting the stepsize amount to a maximum value when the Indicator is above a first threshold value and when

$$|Ones - Zeros| > SecondThreshold\ .$$

21. The method of reducing bit errors according to claim 18, further comprising:

setting the stepsize amount to a minimum value when the Indicator is below a first threshold value; and

setting the stepsize amount to a maximum value when the Indicator is above a

first threshold value and when

$$|Ones - Zeros| > SecondThreshold\ .$$

22. The method of reducing bit errors according to claim 18, further comprising:

setting the stepsize amount to a minimum value when the Indicator is below a first threshold value; and

setting the stepsize amount to a maximum value when the Indicator is above a first threshold value and when

$$TotalCount > ThirdThreshold$$

where TotalCount = Ones + Zeros.

23. The method of reducing bit errors according to claim 21, further comprising:

determining a direction of change to be effected by said adjusting the decision threshold signal.

24. The method of reducing bit errors according to claim 22, further comprising:

determining a direction of change according to a relative number of corrected "1"s and "0"s.